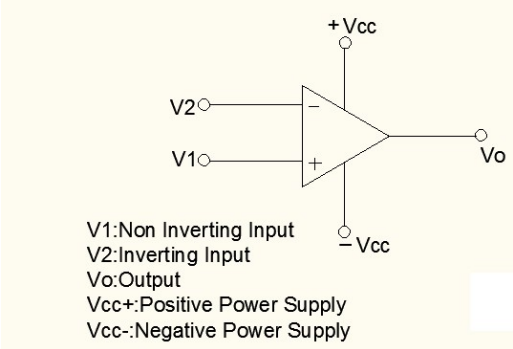
UNIT I
BASIC OPERATIONAL AMPLIFIERS

Operational Amplifiers (IC741)

An operational amplifier is a **direct coupled high gain negative feedback amplifier.** It can amplify the signals in the range of **0 Hz to 1MHz**. It is a basic linear integrated circuit. In analog computers, it is designed to perform mathematics operations like addition, subtraction, differentiation, integration, multiplication, division etc., so, it is called as operational amplifier. IC741 operational amplifier is an 8bit dual in line package IC. It is a very popular type IC. It has **five basic terminals**.

- Two input terminals
- One output terminal
- Two supply terminals

SCHEMATIC SYMBOL FOR OP AMP



It contains Two inputs

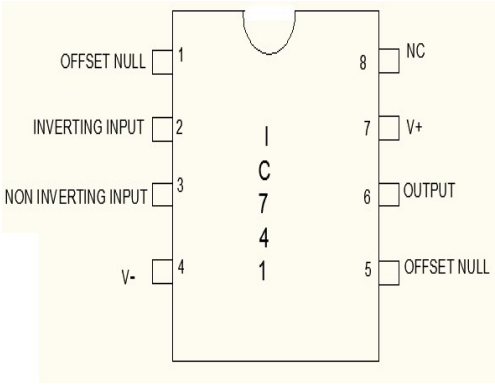
- Inverting input(V1)
- non-inverting input (V2)

Only one output (V0).

A positive and a negative supply voltage are needed for its normal operation**. The signal given to the inverting input in always inverted at its output.** A positive voltage at the inverting input produces a negative output voltage, and similarly a negative input voltage produces a positive output voltage. But the signal given to the non-inverting input will not produce any sign change at the output. The functions of an op-amp generally depends upon the external connected components.

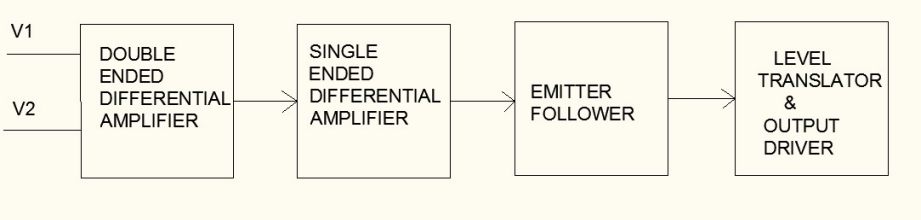
PIN DIAGRAM OF OP-AMP IC 741 IC

741 operational amplifiers are an ***8-pin dual-in-line package IC***. The pin diagram of IC741 is shown in given figure.



- Pin no 1: off-set null balance
- Pin no 2: inverting input
- Pin no 3: non-inverting input
- Pin no 4: Negative supply
- Pin no 5: off-set null balance
- Pin no 6: output
- Pin no 7: positive supply
- Pin no 8: no connection

Block diagram of an OP-AMP:



An op-amp is a high quality amplifier. It contains four stages

- Double ended differential amplifier
- Single ended differential amplifier
- Emitter follower
- Level transistor and output driver.

They are connected in cascaded manner.

Double ended differential amplifier:

This stage provides maximum voltage gain. This stage should employ a current source at the common emitter node for good common mode rejection.

Single ended differential amplifier:

It is also called as intermediate gain stage. It does not require a current source in the emitter. The purpose is to provide some additional gain. In order to prevent excessive loading of the first stage, its input resistance should be relatively high. **Level transistor and output driver** This stage is used to prevent undesired dc current in the load and increasing the permissible output voltage swing. Finally, it produces large output voltage or current.

CHARACTERISTICS OF AN IDEAL OP-AMP:

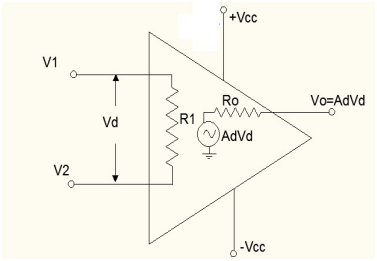
The ideal op-amp is a differential input, single ended output device. The characteristics are as follows.

- High input impedance, Ri = α. (Practically 1 mega ohm)
- Low output impedance, R0 = 0 (Practically 1 to 2 ohm)
- High voltage gain, AV =α (Practically several thousands)
- High bandwidth, BW = α (V restricted by slew rate)
- Perfect balance; V0 =0 when V1= V2.
- Characteristics do not drift with temperature.

Simple equivalent circuit of an op-amp:

The equivalent circuit is nothing but the representation of op-amp parameters in terms of its physical component. The equivalent circuit of an op-amp is shown in given figure.

Equivalent circuit of op-amp:



Here, the op-amp parameters the input resistance, output resistance, open loop voltage gain are represented in terms of circuit components like Ri, R0 etc. The op-amp amplifies the difference between the two input voltages.

$$\mathbf{V_o = A_d V_a = A_d(V_2 - V_2)}$$

Where

A_d = Large signal open loop voltage gain

V_d = differential input voltage

V_1 = inverting input voltage with respect to ground

V_2 = non-inverting input voltage with respect to ground

R_i = input resistance of op-amp

R_0 = output resistance of op-amp

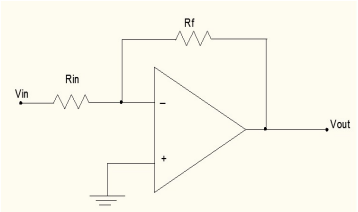
The output voltage is directly proportional to the difference voltage V_d. The op-amp amplifies the difference voltage and not the individual input voltages. Thus the polarity of output signal is decided by the polarity of the difference voltage V_d.

Application of op-amp

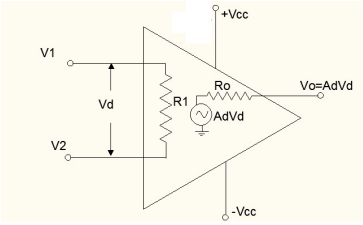
- Audio and video pre-amplifiers and buffers
- Voltage comparators
- Differential amplifiers
- Differentiators and integrators
- Filters
- Precision rectifiers
- Precision Peak Detector

- Voltage and current regulators
- Analogue calculators
- Voltage clamp
- Analog-to-digital converters
- Digital-to-analog converters

VIRTUAL GROUND:



An inverting amplifier is shown in above figure. In this figure, noninverting input is grounded, and the input signal (Vi) is applied to the inverting input terminal through a resistor Ri.



The figure represents equivalent circuit of op-amp.
In general the output voltage of an op-amp
V_0 = Ad Vd = Ad (V2-V1)
A_d = large signal open loop voltage gain
Vd = differential input voltage
V_1 = inverting input voltage with respect to ground
V_2 = non- inverting input voltage with respect to ground
Assuming $V_0 = V_2 - V_1$
$V_d = V_0/A_d$
Since Ad is very large, $V_d = 0$
V1≅ V2

The voltage at the inverting terminal (V_1) is approximately equal to that at the non-inverting terminal (V_2). So, the differential voltage is zero. In other words, the inverting terminal voltage Vs is approximately at ground potential because V_2 is directly connected to ground. That means, the inverting terminal is not directly connected to ground, but it acts like a ground terminal. Therefore, the inverting terminal is said to be at virtual ground.

PARAMETERS OF OP-AMP:

Input offset voltage:

It is the input voltage which should be applied between the input terminals to get zero output voltage.

Input offset current:

It is the difference between the currents entering the inverting and non-inverting input terminals of an operational amplifier.

Input bias current:

It is the average of the currents that enter into the inverting and noninverting input terminals of a operational amplifier.

Output offset voltage:

It is the output voltage present, when the two input terminals are grounded.

Differential input resistance:

It is the equivalent resistance that can be calculated at either the inverting or non-inverting input terminal with the other terminal connected to ground.

Input capacitance:

It is the equivalent capacitance that can be calculated at either the inverting or non-inverting terminal with the other terminal connected to ground.

Open loop voltage gain (Av):

When the op-amp is used without any feedback, the differential voltage gain is known as open loop voltage gain.

Supply voltage rejection ratio (SVRR):

It occurs because of supply voltage variations, which leads to changes in input offset voltage. SVRR is the ratio of the change in input offset voltage to the corresponding change in one power supply voltage, with all remaining power voltages held constant.

Output voltage swing:

It is the maximum peak-to-peak output voltage (+ve or –ve saturation voltage) which can be obtained without waveform clipping when DC output is zero.

Slew rate (SR):

It is defined as the maximum rate of change of output voltage per unit of time. It is expressed in volts per microseconds.

$$\mathbf{SR} = \frac{dv_0}{dt} \mathbf{/maximum}$$

Common mode rejection ratio (CMRR)

CMRR is the ratio of differential voltage gain (Ad) to the common mode voltage gain (Acm).

$$\mathbf{CMRR} = \frac{A_d}{A_{cm}}$$

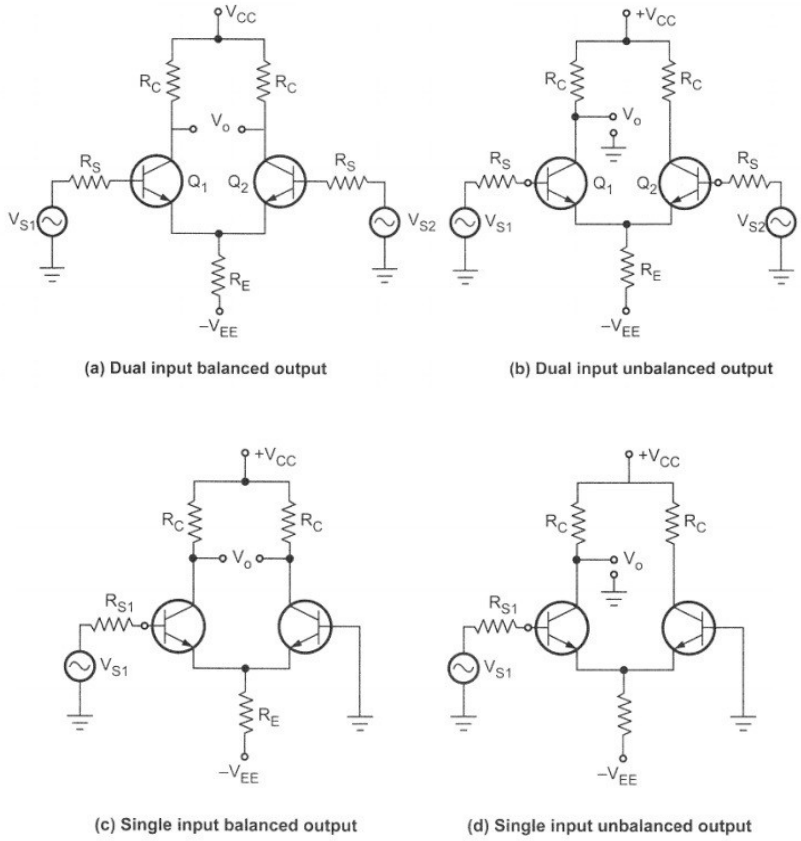
Maximum differential input voltage:

It is the maximum value of differential input voltage that can be applied without damaging the op-amp.

Maximum common mode input voltage:

It is the maximum voltage to which that the two inputs can be raised above ground potential before the op-amp.

Basic Concept of Differential Amplifier



A differential amplifier is a type of electronic amplifier which multiplies the difference between two inputs by some constant factor. It is the basic building block of an OPAMP. The two transistors Q_1 and Q_2 have identical characteristics. The intensity of +VCC is equal to the intensity of –VEE. These voltages are measured with respect to ground. Ideally, the output voltage is zero when the two inputs are equal. In an equation form, V0 ∞ VS1 ~ VS2.

There are four configurations of a differential amplifier, shown in Figure

(a) Dual input balanced output differential amplifier

- The signal is given to both the input terminals
- The output is taken between the two collectors

(b) Dual input, unbalanced output differential amplifier.

- The signal is given to both the input terminal
- The output is taken from one collector with respect to ground

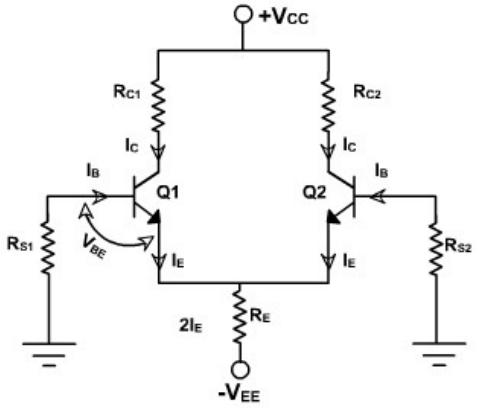
(c) Single input, balanced output differential amplifier.

- The signal is given to only one input terminal and another terminal is grounded
- The output is taken between the two collectors

(d) Single input, unbalanced output differential amplifier

- The signal is given to only one input terminal and another terminal is grounded
- The output is taken from one collector with respect to ground

DC Analysis of a Dual input – Balanced Input Differential Amplifier



Since the emitter biased part is common for both the sections as shown in Figure, therefore determining the operating point for only one section will be applicable for both the sections.

As the value of R_{S1} and R_{S2} are equal, let us take $R_{S1} = R_{S2} = R_S$.

Applying KVL in the base emitter loop of the first section,

$R_{S1}B = V_{BE} + 2I_ER_E = V_{EE}$

But $I_B = I_C/\beta_{dc}$ and $I_C = I_E$ ------→ (1)

Therefore, $R_{SI}C / \beta_{dc} + V_{BE} + 2I_ER_E = V_{EE}$

Or $I_C = I_E = (V_{EE} – V_{BE}) / (2R_E + R_S / \beta)$

Generally, $R_S/\beta_{dc} << 2R_E$ as R_S is the internal resistance of the input signal

Therefore $I_C = I_E = (V_{EE} – V_{BE}) / 2R_E$ -----→ (2)

Again $R_{C1} = R_{C2} = R_C$

Applying KVL in the collector emitter loop, $V_{CC} = I_CR_C + V_{CE} + 2I_ER_E – V_{EE}$

Or $V_{CE} = V_{CC} – I_CR_C – (2I_ER_E – V_{EE})$ ----→ (3)

Now, if R_S is negligible, from (1)

$V_{BE} = 2I_ER_E – V_{EE}$ ----------→ (4)

Thus, applying (4) in (3) we get

$V_{CE} = V_{CC} – I_CR_C - V_{BE}$

Or , $V_{CE} = V_{CC} – V_{BE} – I_CR_C$ ------→ (5)

I_CQ and $V_{CE}Q$ can be determined from (2) and (5) respectively

Constant Current Bias

In the DC analysis of the differential amplifier, it was observed that emitter current IE depends on the value of the β. To make the operating point stable, IE current should be constant irrespective of the value of β. To avoid the effect of β, RE should be quite large. But a large value of RE in turn decreases the current IE and then, to maintain the same value of IE, emitter supply VEE should be increased. But as it is not a practical way out, another technique, called the current bias is used.

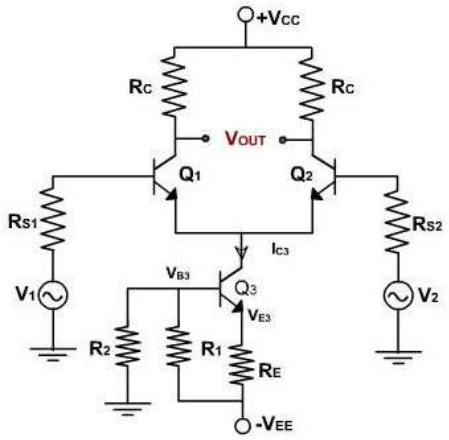


Figure shows dual input balanced output differential amplifier by using a constant current bias. The resistance R_E can be replaced by the constant current transistor Q_3. The DC collector current in Q_3 can be established by R_1, R_2, & R_E.

By applying the voltage divider rule, the voltage at base of Q_3 is

$$V_{B3} = \frac{R_2}{R_1 + R_2}(-V_{EE})$$

$$V_{E3} = V_{B3} - V_{BE3}$$

$$= -\frac{R_2}{R_1 + R_2} V_{EE} - V_{BE3}$$

$$I_{BE3} = I_{C3} = \frac{V_{E3} - (-V_{EE})}{R_E}$$

$$= \frac{V_{EE} - \left(\frac{R_2}{R_1 + R_2}\right) V_{EE} - V_{BE3}}{R_E}$$

As the two halves of differential amplifiers are symmetrical, each has half of the current IC3.

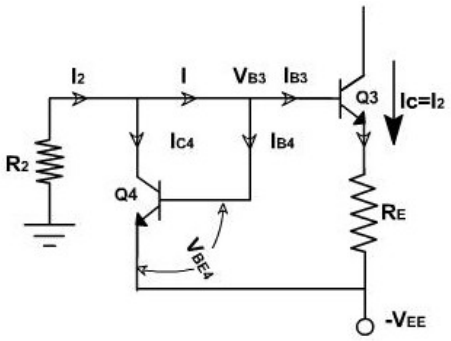
$$I_{E1} = I_{E2} = \frac{I_{C3}}{2} = \frac{V_{EE} - \left[\frac{R_2}{R_1 + R_2} V_{EE}\right] - V_{BE3}}{2R_E}$$

The collector current, I_C3 in transistor Q_3 is fixed as no signal is injected into either the emitter or base of Q_3.

Besides supplying the constant emitter current, constant current bias provides a very high source resistance also since the AC equivalent or DC source is ideally an open circuit.

Current Mirror

The circuit in which output current is forced to equal the input current is said to be a current mirror circuit. Therefore, in a current mirror circuit, the output current is a mirror image of input current. The current mirror circuit is shown in the figure



The current mirror is the special case of constant current bias. The current mirror bias requires few components than the constant current bias circuits. As Q_3 and Q_4 are identical transistors,

$$V_{BE3} = V_{BE4}$$

$$I_{B3} = I_{B4}$$

$$I_{C3} = I_{C4}$$

Summing currents at node V_{B3}

$$I_2 = I_{C4} + I$$

$$= I_{C4} + 2I_{B4} = I_{C3} + 2I_{B3}$$

$$= I_{C3} + 2\left(\frac{I_{C3}}{\beta_{dc}}\right)$$

$$= I_{C3}\left(1 + \frac{2}{\beta_{dc}}\right)$$

Generally β_{dc} is large enough, therefore $2/\beta_{dc}$ is small.

$$\therefore I_2 \approx I_{C3}$$

$$I_2 = \frac{V_{EE} + V_{BE3}}{R_2}$$