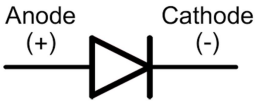
UNIT – I

Power Semiconductor Diodes and Transistors

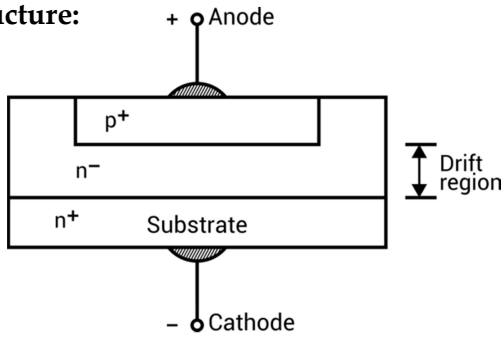
Power diodes

Power diodes carry high currents, withstand high reverse voltages and should possess fast switching characteristics. Power diode is uncontrolled device.

Symbol:



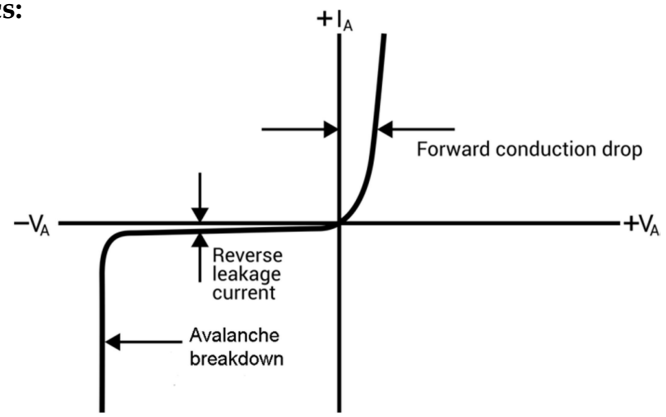
Structure:



Description:

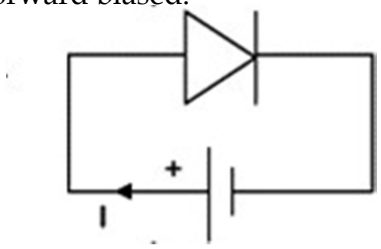
Power diode consists of three layers. The bottom layer is heavily doped n^+ substrate. On n^+ substrate n^- layer is epitaxially grown. On other side n^+ substrate that forms cathode of the diode. The n^- layer is known as a drift region and is lightly doped. The drift region determines the breakdown voltage of the device. Now heavily doped P^+ layer is diffused into n^- layer to form anode.

VI Characteristics:



Forward Characteristics:

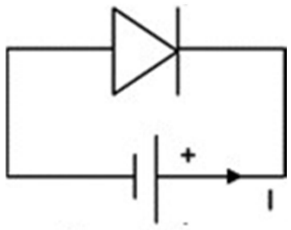
When the anode potential is positive with respect to cathode, the diode is said to be forward biased.



Under forward-bias condition, the forward diode current is very small up to cut in voltage. Cut in voltage is also known as threshold voltage or turn on voltage. Beyond the cut in voltage, the forward current increases rapidly and diode conducts fully.

Reverse Characteristics:

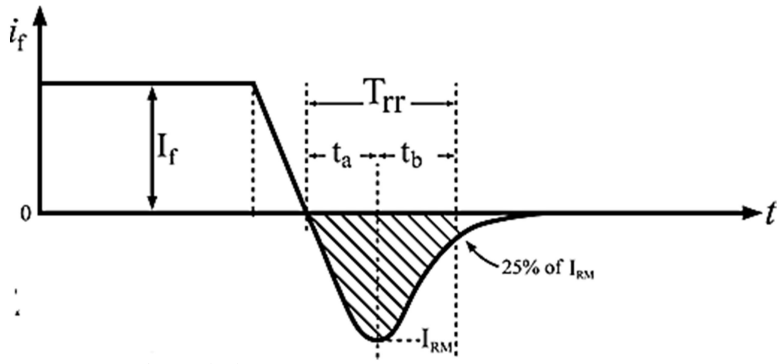
When the cathode potential is positive with respect to anode, the diode is said to be reverse biased.



A very small amount of leakage current flows in the reverse bias. The leakage current increases slowly with reverse voltage until breakdown or avalanche voltage is reached. At this voltage, diode is turned on in the reverse direction. Once the reverse breakdown occurs, the reverse current increases drastically with small increase in reverse voltage

Reverse Recovery Characteristics:

Reverse Recovery Characteristics of Diode is actually the Turn-off transient portion of the Switching Characteristics. When the diode is conducting in forward conduction mode, to turn it off, reverse voltage is applied. When the reverse voltage is applied, the forward diode current (I_F) decreases linearly to zero, the diode continues to conduct in the reverse direction. The reverse current flows for a time called reverse recovery time t_{rr}.



Reverse Recovery time (t_{rr}) :

Total time taken by the reverse recovery current (I_{RM}) to reach 25% of its maximum value is called Reverse Recovery time (t_{rr}).

$$t_{rr} = t_a + t_b$$

t_a : Time is taken by the reverse recovery current to become maximum I_{RM}.

t_b : Time is taken by the reverse recovery current to decreases to 25% of its maximum value.

Softness Factor (S):

The softness factor is also called as S-factor.

$$\text{Softness factor } S = t_a / t_b$$

If the softness factor is equal to 1 then such a diode is called soft recovery diode. If the softness factor is less than 1 then such a diode is called fast recovery diode.

Power BJT

A Power BJT is Current controlled device. The word "transistor" is derived from the words "Transfer" and "Resistor". It's called "bipolar" because the conduction takes place due to both electrons as well as holes.

Types:

- NPN transistor
- PNP transistor

Symbol:

NPN transistor **PNP transistor**

Transistor Terminals:

The three terminals of transistor is Emitter, Base and Collector

Structure:

Construction:

The n^+ Emitter region is heavily doped. The P type Base region is lightly doped and very thin. The thickness of base provides good amplification capabilities. The n^+ collector is split into two regions n^+, n^-. The n^- region is lightly doped and it is called collector drift region. The thickness of n^- region determines the breakdown voltage capabilities of transistor. The n^+ collector region is heavily doped.

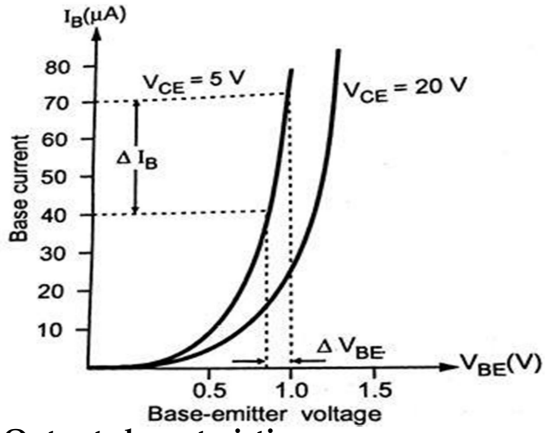
Steady State Characteristics:

i) Input Characteristics
ii) Output Characteristics

Input characteristics:

Input Characteristics is the graph drawn between Base current (I_B) and base Emitter voltage (V_{BE}) for constant Collector Emitter voltage (V_{CE}).

Model graph:

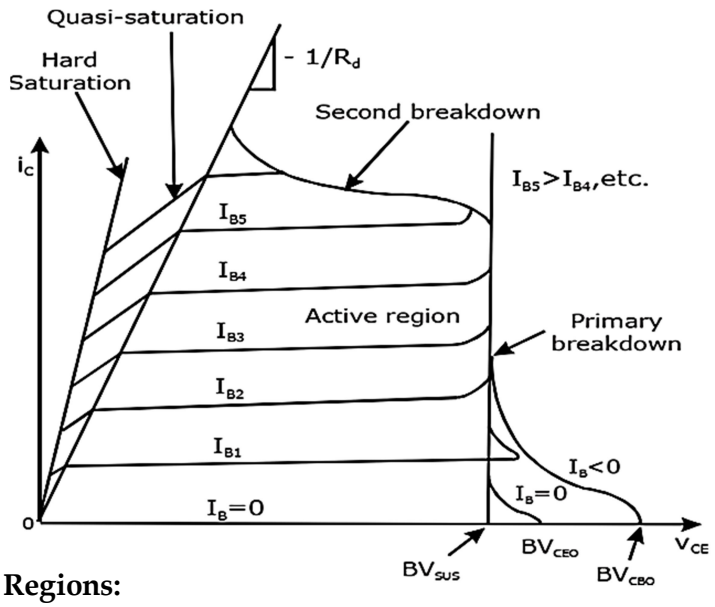


Description:

- Collector Emitter voltage (V_{CE}) is kept constant at particular value.
- Base Emitter voltage (V_{BE}) is increased in steps and note down corresponding Base current (I_B)
- The procedure is repeated for different values of Collector Emitter voltage (V_{CE})

Output characteristics:

Collector current (I_c) versus Collector Emitter voltage (V_{CE}) are drawn for constant Base current (I_B)



BV_{SUS} is the maximum collector to emitter voltage when BJT is carrying substantial collector current.

BV_{CEO} is the maximum collector to emitter breakdown voltage when base current is zero.

BV_{CBO} is the maximum collector to base breakdown voltage when emitter current is zero.

Regions:

The output characteristics have four regions

i) Cut off region **ii) Active region**
iii) Quasi Saturation region **iv) Hard Saturation region**

Cutoff region:

The cutoff Region is the area where base current is almost is zero. Hence no collector current flows and transistor is said to be OFF.

Active region:

The power BJT is never operated in the active region (i.e. as an amplifier) and it is always operated between cut-off and saturation.

Quasi Saturation region:

When BJT operates at high frequency, it is operated in this region. In Quasi Saturation the base drive is applied and transistor is said to be ON.

Hard Saturation region:

Hard Saturation region is also known as deep saturation region. In Hard Saturation the base drive is applied and transistor is said to be ON. It needs more time to turn off. So, this region is suitable only for low-frequency switching application.

Primary breakdown:

The primary breakdown in BJT takes place due to avalanche breakdown of the collector base junction. The large power dissipation leads to primary breakdown.

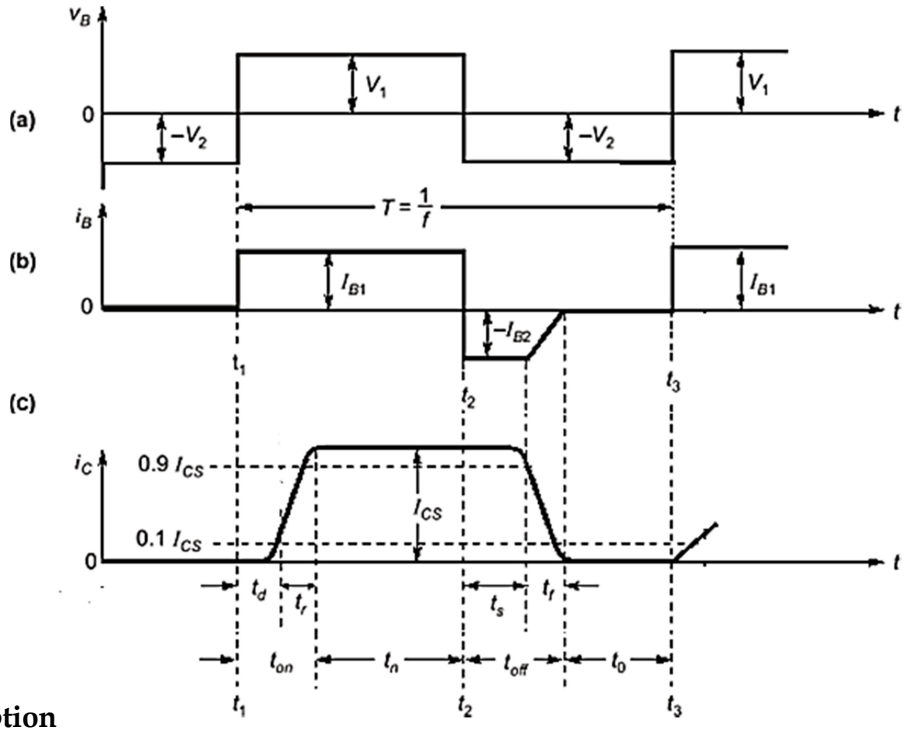
Secondary breakdown:

At the large collector currents, the collector emitter voltage drops. Hence there is an increase in power dissipation. Therefore the temperature increases very rapidly and the BJT is damaged.

Switching characteristics

For switching applications, Power BJT is operated only in Saturation and cutoff region.

Switching waveform



Description

- Turn on time (ton)
- Turn off time (toff)

(i) Turn on time (ton):-

The time required to turn on the Power BJT, when the Base Emitter Voltage (V_{BE}) and Base current (I_B) is made positive.

Turn on time (ton) = td+tr

Delay time (td):-

Delay time is defined as the time during which the collector current rises from zero to 0.1 I_{CS}

Rise time (tr):-

Rise time is defined as the time during which the collector current rises from 0.1 I_{CS} to 0.9 I_{CS}

(ii) Turn off time (toff):-

The time required for the Base Emitter Voltage (V_{BE}) and Base current (I_B) are reversed to turn off the Power BJT.

Turn off time (toff) = ts+tf

Storage time (ts):-

Storage time is defined as the time during which the collector current falls from I_{CS} to 0.9 I_{CS}.

Fall time (tf):-

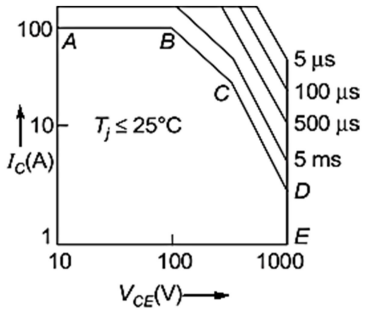
Fall time is defined as the time during which the collector current drops from 0.9 I_{CS} to 0.1 I_{CS}.

Safe Operating Area:

The Safe Operating area of a power transistor specifies the safe operating limits of collector current (I_C) versus collector emitter voltage (V_{CE}). For reliable operation of the transistor, collector current and voltage must always lie within this area.

Forward Biased Safe Operating Area (FBSOA)

A Plot of collector current (I_C) versus collector emitter voltage (V_{CE}) when the base emitter junction is forward biased to turn on the transistor.

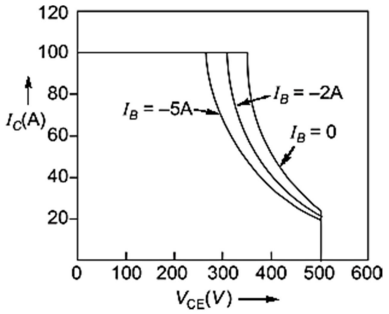


FBSOA for power transistor (logarithmic scale)

AB: Maximum limit for dc and continuous current
BC: To limit junction temperature to safe value
CD: Secondary breakdown limit
DE: Maximum voltage capability

Reverse Biased Safe Operating Area (RBSOA)

A Plot of collector current (I_C) versus collector emitter voltage (V_{CE}) when the base emitter junction is reverse biased to turn off the transistor.



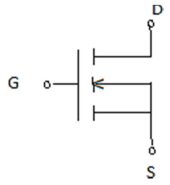
- Specifies the limits of transistor operation at turn off when the base current is zero or when the base emitter junction is reverse biased.

With increased reverse bias, area of RBSOA decreases in size.

Power MOSFET

The Metal Oxide Semiconductor Field Effect Transistor has been developed by combining the areas of field effect concept and MOS technology. The Power MOSFETs are majority carrier device. (i.e.) Its current conduction is due to majority carriers only. PMOSFET is a Voltage Controlled Device.

Symbol:



A Power MOSFET has three terminals:
Drain (D),
Source(S),
Gate (G).

Types:-

There are two types of P-MOSFET,

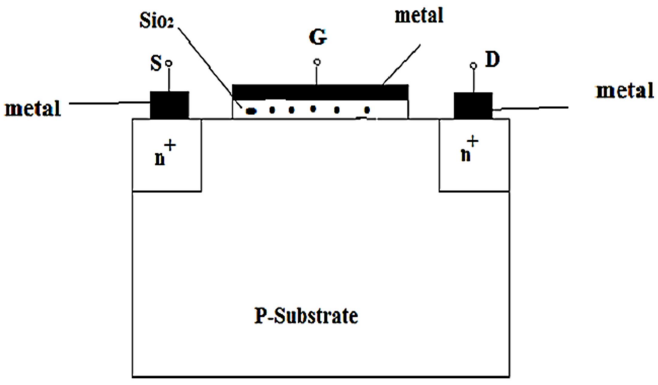
1. Enhancement mode P-MOSFET **2.** Depletion mode P-MOSFET.

In both of these types the MOSFETs can be N-channel or P-channel.

Structure:

The P-MOSFET has only one P-region. This region is called substrate.

Circuit diagram:



Construction:

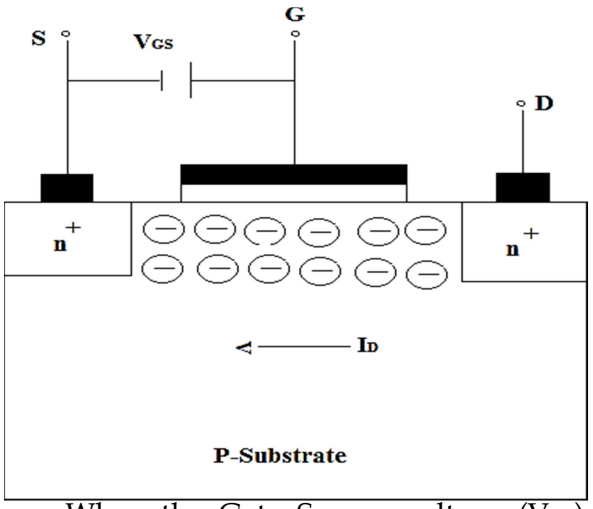
The Source and Drain are connected to n+ regions. The n+ regions are heavily doped. The Gate is not directly connected to P-substrate. There is an oxide layer (Sio_2) between Gate terminal & P-Substrate. The oxide layer acts as an insulating medium between Gate & P-Substrate. Hence P-MOSFET is also called as Insulated Gate FET (IGFET).

Working: -

(i) Enhancement Mode P-MOSFET: -

When the Gate Source voltage (V_{GS}) is positive, the device is operated in Enhancement Mode.

Circuit Diagram



Construction

When the Gate Source voltage (V_{GS}) is positive, an accumulation layer of electrons is formed in the P-substrate near oxide layer. This is also called induced channel of electrons. Therefore current (I_D) start flowing through this induced channel. The current flows from Drain to Source. Since the channel is made of electrons, this is called N-channel.

When the Gate Source voltage (V_{GS}) is further increased, an induced N-channel deeper. This enhances the conduction process of the channel. (ie) More current (I_D) flows from drain to Source. In Enhancement mode P-MOSFET, the Drain current (I_D) enhanced by Gate Source voltage (V_{GS}).

(ii) Depletion Mode PMOSFET:-

When the Gate Source voltage (V_{GS}) is Negative, the device is operated in Depletion mode P-MOSFET. The transistor requires the Gate-Source voltage (V_{GS}) to switch the device OFF.

When the Gate Source voltage is reduced and made negative, an accumulation layer of holes is formed in the N-channel. (ie) It creates depletion layer which reduces the conduction of Drain current (I_D).

Pinch off voltage:-

As Gate Source is further reverse biased, the complete channel is depleted and no current flows from Drain to Source. The Gate Source voltage at which this happens is called Pinch off voltage of P-MOSFET.

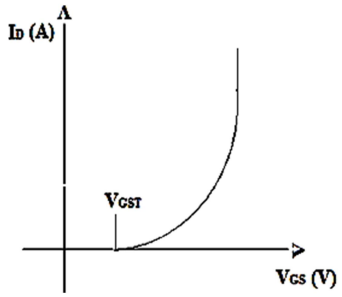
Static characteristics of P-MOSFET:-

The Static characteristics of P-MOSFETs are,

i) Transfer characteristics
ii) Output characteristics

(1) Transfer characteristics:-

The Drain current (I_D) is plotted with Gate Source voltage (V_{GS}) for constant Drain Source (V_{GS}) voltage.



i) When $V_{GS} > V_{GST}$, Drain current (I_D) increases heavily

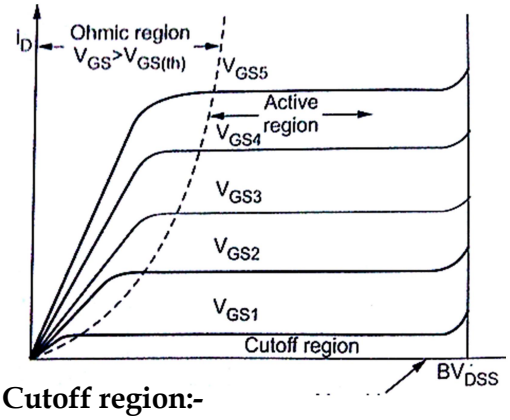
ii) Below V_{GST}, the device is in OFF state.

iii) V_{GST} -Threshold Gate Source voltage

The V_{GST} is the minimum positive gate source voltage.

(2) Output characteristics:-

The Drain current (I_D) is plotted with Drain Source voltage (V_{DS}) for various values of Gate source voltage (V_{GS}).



The three regions are,

- Cut off region
- Ohmic region
- Active region

Cutoff region:-

The PMOSFET is driven into Cutoff Region when $V_{GS} < V_{GST}$.

Where V_{GST} -Threshold Gate Source voltage.

In the cut off region the drain current is Small. Therefore it is negligible and P-MOSFET is said to be in OFF State.

Ohmic region:-

The P-MOSFET is driven into ohmic region when $V_{GS} >> V_{GST}$. In the ohmic region, the MOSFET conducts heavily. Hence it is said to be 'ON' in the ohmic region.

Active region:-

The power MOSFET is never operated in the active region (i.e. as an amplifier) and it is always operated between cut-off and saturation.

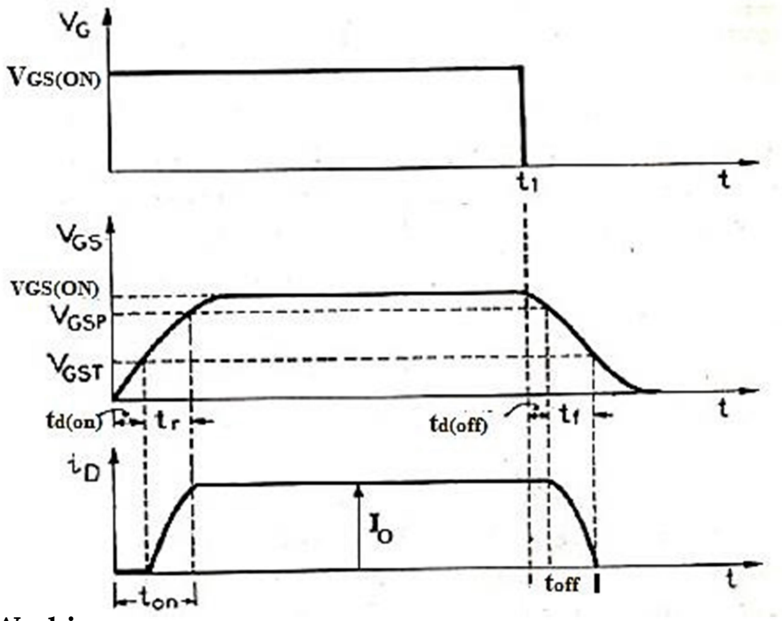
BV_{DSS}:-

The BV_{DSS} is the Drain to Source breakdown voltage, when the Gate is open circuited. The P-MOSFET is damaged if Drain to Source voltage is increased above BV_{DSS}.

Switching characteristics of P-MOSFET:-

The internal capacitances of P-MOSFET affect the turn on and turn off times of P-MOSFET. C_{gs} is the Gate Source capacitance. For switching applications, P-MOSFET is operated only in ohmic and cutoff region.

Switching Waveform



Working:

(i) Turn on time (ton)
(ii) Turn off time (toff)

(i) Turn on time (ton):-

The Voltage is applied between Gate-Source to turn on the P-MOSFET.

Turn on time (ton) = td(on) +tr

Turn on delay time (td(on)):-

The turn on delay time is the time required to charge C_{gs} to threshold Gate Source voltage V_{GST}.

Where V_{GST} – Threshold Gate Source voltage.

After this voltage, the drain current (I_D) starts Increasing.

Rise time (tr):-

The time required for charging Cgs from V_{GST} to V_{GSP}.

V_{GSP} – Pinch off region Gate Source voltage.

The Drain current rises to its maximum value (I_D). The P-MOSFET is then said to have fully turned on condition.

(ii) Turn off time (toff):-

To turn off the P-MOSFET, the Gate voltage is removed.

Turn off time (t_{off}) = $t_{d(off)} + t_f$

Turn off delay time (td(off)):-

Turn off delay time is the time is required for discharging Cgs from $V_{GS(on)}$ to V_{GSP}.

$V_{GS(on)}$ -> Overdrive Gate voltage

The Drain current (I_D) start reducing.

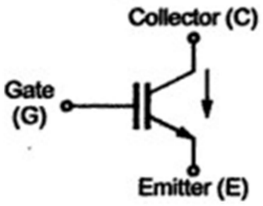
Fall time (tf):-

The Fall time is the time required for discharging Cgs from V_{GSP} to V_{GST}. The Drain current reduces to Zero. The Drain current becomes zero when $V_{GS}<V_{GST}$. The PMOSFET is then said to have turned off. The Cgs then discharges to zero.

IGBT :(Insulated Gate Bipolar Transistor)

The Insulated Gate Bipolar Transistor (IGBT) has been developed by combining the properties of BJT and PMOSFET. The IGBT is a Majority carrier device. (i.e.) Its current conduction is due to majority carriers only. IGBT is a Voltage Controlled Device.

Symbol:-



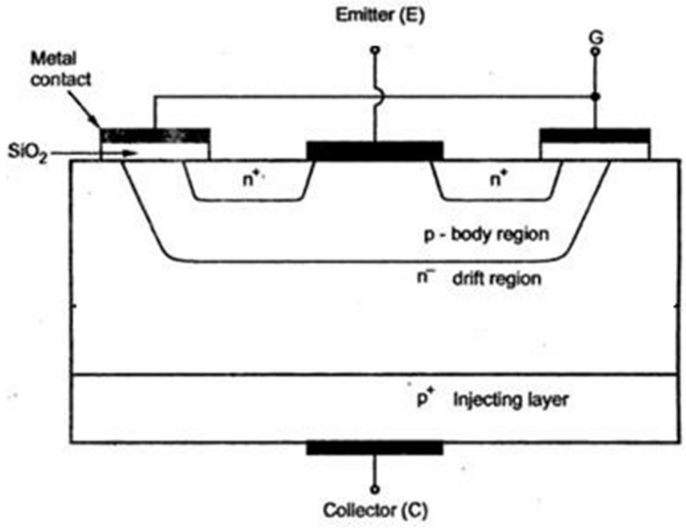
The IGBT has three terminals:

i.Gate (G)

ii.Collector (C)

iii.Emitter (E)

Structure of IGBT:-

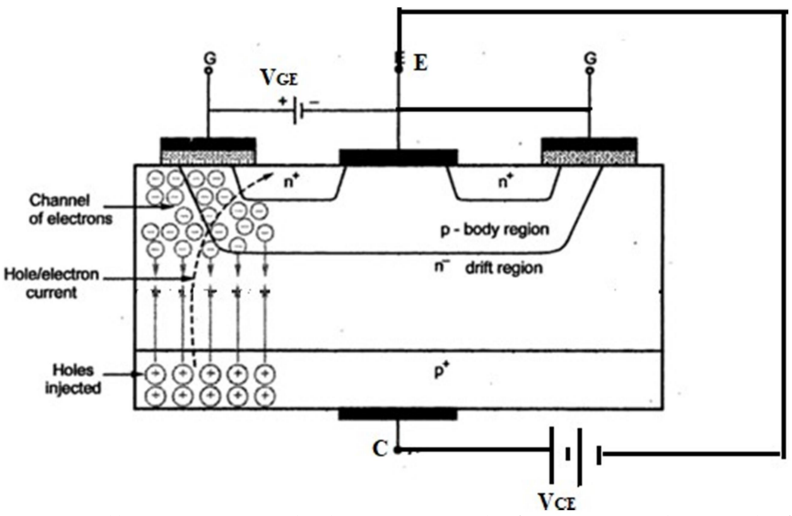


Construction:-

In IGBT p+ layer is used as substrate. The p+ substrate is called as collector. The p+ substrate is also called as injection layer because holes injected into n^- layer. The p+ substrate is heavily doped. The n^-layer is called as drift region. The n^- drift region is lightly doped. The thickness of n^- layer determines the voltage blocking capability of IGBT. The P layer is called as body region of IGBT.

The p+, n^- layer are joined to form junction j_1 .The p, n^- layer are joined to form junction j_2 .The p n+ layer are joined to form junction j_3.

Working:-



Description:-

When gate emitter voltage is positive with $V_{GE}>V_{GET}$, an n channel is induced in the p body region.

$\mathbf{V_{GET}} \rightarrow$ Threshold gate Emitter voltage.

Electrons flow from n+ Emitter to n-drift region through the n channel. As IGBT is forward biased with Collector positive and Emitter negative, p+ collector injects holes into n- drift region. The n- drift region is filled with electrons from p Layer and holes from p+ collector region. $\therefore$ Injection carrier density in drift region increases and as a result, conductivity of n-layer increases that enhances collector current Ic significantly therefore IGBT get turned on and begins to conduct.

With No voltage between Gate and Emitter, junction J_2 is reverse biased. So no current flows from Collector to Emitter. Therefore IGBT gets turned off

Static characteristics (IV Characteristics):-

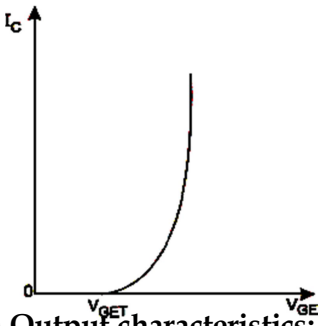
The Static characteristics of IGBTs are,

➡Transfer characteristics ➡Output characteristics

(1) Transfer characteristics:-

The Collector current (Ic) is plotted with Gate Emitter voltage (V_{GE}) for constant Collector Emitter (V_{CE}) voltage.

Model Graph



i) When $V_{GE}> V_{GET}$, Collector current (Ic) increases heavily.

ii) Below V_{GET}, the device is in OFF state.

V_{GET} -Threshold Gate Emitter voltage.

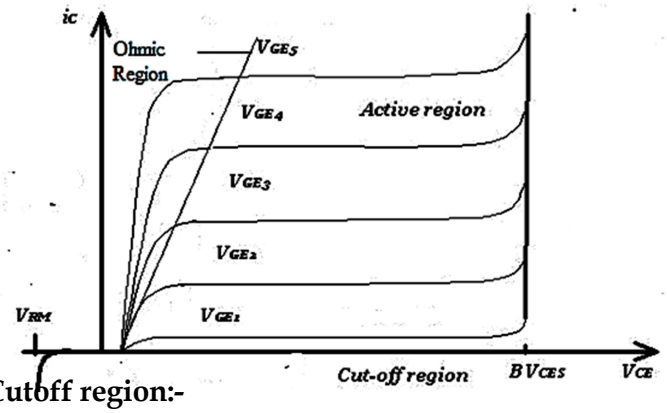
The V_{GET} is the minimum positive gate Emitter voltage.

(2) Output characteristics:-

The Collector current (I_c) is plotted with Collector Emitter voltage (V_{CE}) for values of Gate Emitter voltage (V_{GE}). $V_{RM} \rightarrow$ max. Reverse Breakdown voltage.

The three regions are, Cut off region, Ohmic region, Active region

Model Graph



BV_{CEE}:- The BV_{CEE} is the Collector to Emitter breakdown voltage, when the Gate is open circuited. The IGBT is damaged if Collector to Emitter voltage is increased above BV_{CEE}.

Cutoff region:-

The IGBT is driven into Cutoff Region when $V_{GE} < V_{GET}$.

Where V_{GET} -Threshold Gate Emitter voltage.

In the cut off region the Collector current is small. Therefore, it is negligible and IGBT is said to be in OFF State.

Ohmic region: -

The IGBT is driven into ohmic region when $V_{GE} >> V_{GET}$. In the ohmic region, the IGBT conducts heavily. Hence it is said to be 'ON' in the ohmic region.

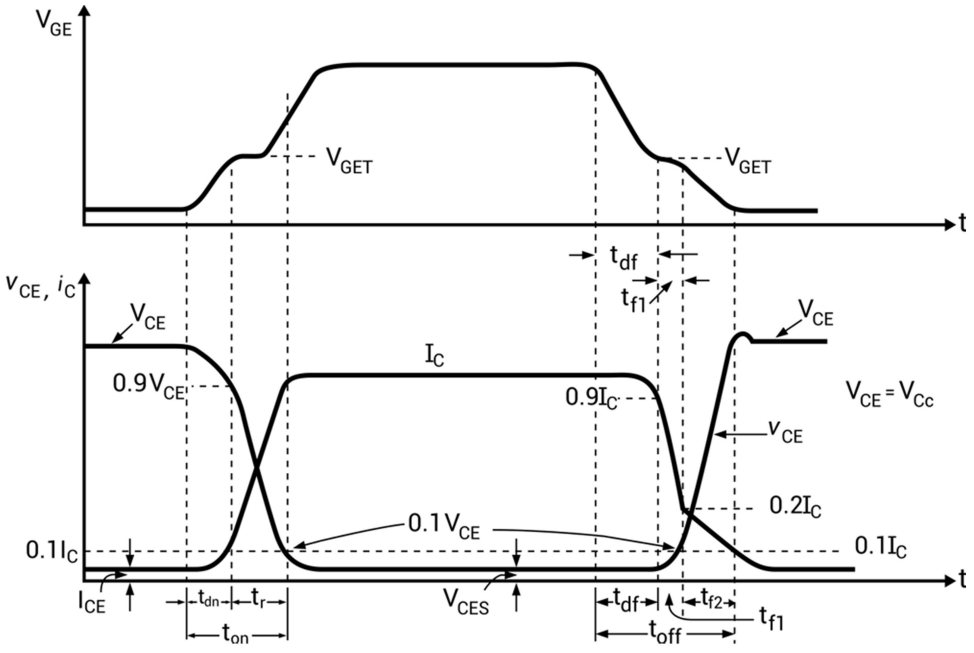
Active region:-

The IGBT is never operated in the active region (i.e. as an amplifier) and it is always operated between cut-off and saturation.

Switching characteristics:-

For switching applications, IGBT is operated only in ohmic and cutoff region.

Switching Waveform



Working

i) Turn on time (ton) ii) Turn off time (toff)

Turn on time (ton):-

The Gate Emitter voltage is made positive to turn on IGBT.

Turn on time (ton) = td(on) +tr

Turn on delay time(td(on)):-

Turn on delay is defined as the time for the Collector-Emitter voltage reduces from V_{CE} to $0.9V_{CE}$. V_{CE} – Initial Collector Emitter Voltage.

It is also defined as the time for collector current to rise from its initial leakage current I_{CE} to 0.1 I_C.

I_{CE} - Initial Collector Emitter Current.

I_C- Final value of Collector Current.

Rise time (tr):-

Rise time is the time during which Collector-Emitter voltage falls from $0.9V_{CE}$to $0.1V_{CE}$. It is also defined as the time for the Collector current to rise from $0.1I_C$ to its finial value I_C.

After time t_{ON} the collector Emitter voltage V_{CE} drops to V_{CES}.

V_{CES}– Conduction drop.

Turn off time (toff):-

The Gate Emitter voltage (V_{CE}) is removed to turn off IGBT.

Turn off time (t_{off}) = $t_{d(off)} + t_{f1} + t_{f2}$

Turn off delay time (td(off):-

The turn off delay time is the time during which the Collector current falls from I_C to 0.9 I_C. At the same time gate voltage begins to rise.

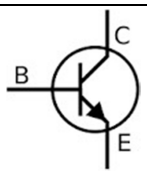
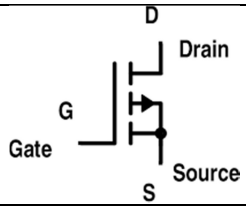
First fall time (t_{f1})

The first fall time is the time during which Collector current falls from 0.9 I_C to 0.2 I_C and Collector Emitter voltage increases to 0.1 V_{CE}.

Final fall time (t_{f2})

The final fall time is the time during which Collector current falls from 0.2 I_C to 0.1 I_C and Collector Emitter voltage increases from 0.1 V_{CE} to V_{CE}.

Comparison between Power BJT with Power MOSFET

Properties	Bipolar Junction Transistor (BJT)	Metal Oxide Semiconductor Field Effect Transistors (MOSFET)
Classification	MOSFETs are categorized into NPN and PNP.	MOSFETs are categorized into enhancement MOSFET (p channel and n channel) and depletion MOSFET (p channel and n channel).
Symbol		
Terminals	Base, Emitter and Collector	Gate, Source and Drain
Transistor type	Bipolar transistor	Unipolar transistor
Charge carriers	Both electrons and holes act as charge carries in BJT.	Either electrons or holes act as charge carrier.
Control method	A BJT is a current controlled device.	A MOSFET is a voltage controlled device.
Switching speed	slow	fast
Input Impedance	Low	High
Output Impedance	Low	Medium
Switching losses	High	Low
Cost	Low	High
Temperature coefficient and paralleling	BJTs have negative temperature coefficient that limits their parallel operation.	MOSFETs have positive temperature coefficient and can be easily paralleled.
Power consumption	A PBJT consumes more power than a PMOSFET.	A PMOSFET Consumes less power than a PBJT.
Secondary breakdown	Secondary breakdown occurs in PBJT	Secondary breakdown doesn't occurs in PMOSFET
Applications	PBJT is preferred for the low current applications. It is widely used as amplifiers, oscillators and electronic switches.	PMOSFET is suitable for high power applications. It is used in power supplies, etc.