Three ways to Reset

- System Reset
- Power Reset
- RTC Domain Reset

System Reset

What happens during System reset ?

- Except for the RTC, RTC backup registers and control/status register, RCC_CSR , all the Registers are reset to their reset values.

How is System Reset Generated ?

- 1. A low level on the NRST pin (external reset)
- 2. Window watchdog end-of-count condition (WWDG reset)
- 3. Independent watchdog end-of-count condition (IWDG reset)
- 4. A software reset (SW reset)

- 5. Low-power management reset
- 6. Option byte loader reset
- 7. Exit from Standby mode

The reset source can be identified by checking the reset flags in the control/status register, RCC_CSR

Software Reset

The SYSRESETREQ bit (Application Interrupt and Reset Control Register) must be set to force a software reset on the device.

Low-power management reset

Two ways to generate low power management reset

- Reset generated when entering Stand By Mode

nRST_STDBY

- Reset when entering Stop mode

nRST_STOP

- 1. Reset generated when entering Standby mode:

  This type of reset is enabled by resetting nRST_STDBY bit in user option bytes.

  whenever a Standby mode entry sequence is successfully executed, the device is reset instead of entering Standby mode.

- 2. Reset when entering Stop mode:

  This type of reset is enabled by resetting nRST_STOP bit in user option bytes.

  whenever a Stop mode entry sequence is successfully executed, the device is reset instead of entering Stop mode.

Option byte loader reset

- The Option byte loader reset is generated when the OBL_LAUNCH bit (bit 18) is set in the FLASH_PECR register.

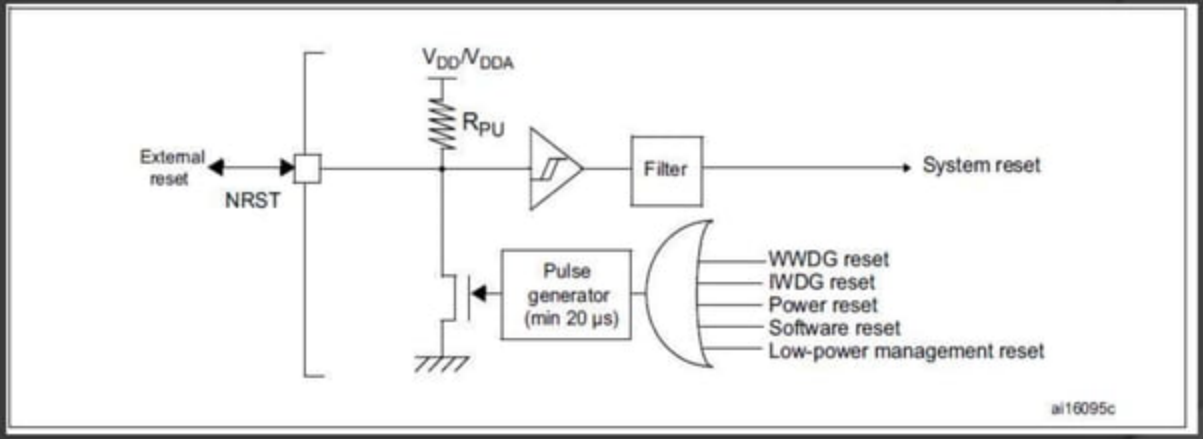
Power Reset

- 1. Power-on/power-down reset (POR/PDR reset)
- 2. BOR reset

What happens During Power Reset ?

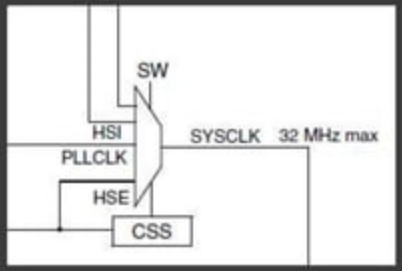
A power reset sets all registers to their reset values including for the RTC domain

Diagram for Reset Circuit



Clocks

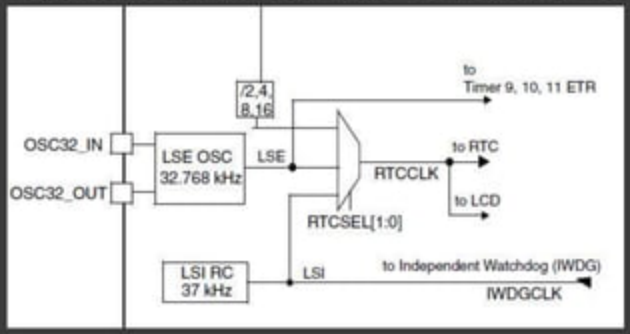
- HSI ((high-speed internal) oscillator clock
- HSE (high-speed external) oscillator clock
- PLL clock
- MSI (multispeed internal) oscillator clock



Secondary Clock

- 37 kHz low speed internal RC (LSI RC) which drives the independent watchdog and optionally the RTC used for Auto-wakeup from Stop/Standby mode.

- 32.768 kHz low speed external crystal (LSE crystal) which optionally drives the realtime clock (RTCCLK)



Each clock source can be switched on or off independently when it is not used, to optimize power consumption.

HSE

- The high speed external clock signal (HSE) can be generated by

HSE external crystal/ceramic resonator

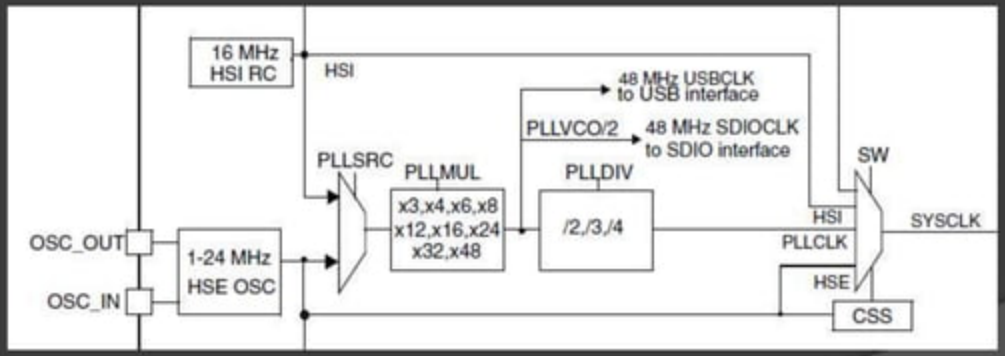
The resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion

HSE

- The 1 to 24 MHz external oscillator has the advantage of producing a very accurate rate on the main clock.
- The HSERDY flag of the RCC_CR register indicates whether the HSE oscillator is stable or not
- An interrupt can be generated if enabled in the *RCC_CR register.*
- The HSE Crystal can be switched on and off using the HSEON bit in the *RCC_CR register.*

HSI

- The HSI clock signal is generated from an internal 16 MHz RC oscillator. It can be used directly as a system clock or as PLL input.



Advantages of HIS

- Low cost ,(No External Components)
- faster startup time than the HSE crystal oscillator

Disadvantage of HIS

- Less accurate than an external crystal oscillator or ceramic resonator.

MSI

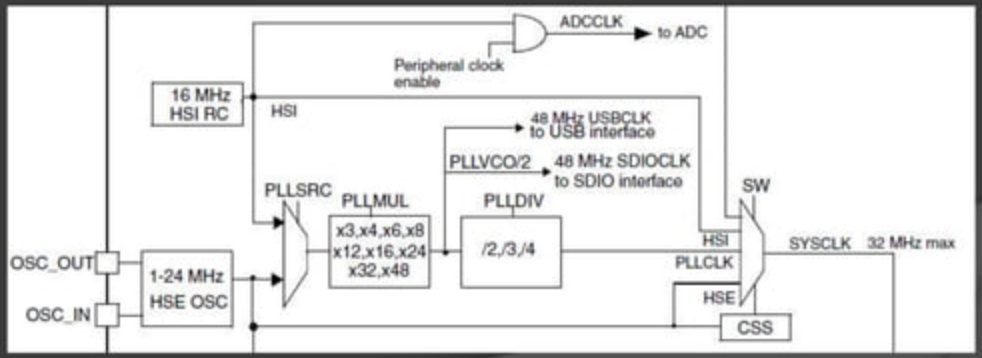
- The MSI clock signal is generated from an internal RC oscillator.
- Its frequency range can be adjusted by software by using the MSIRANGE[2:0] bits in the RCC_ICSCR register.
- Seven frequency ranges are available: 65.536 kHz, 131.072 kHz, 262.144 kHz, 524.288 kHz, 1.048 MHz, 2.097 MHz (default value) and 4.194 MHz.

Advantages

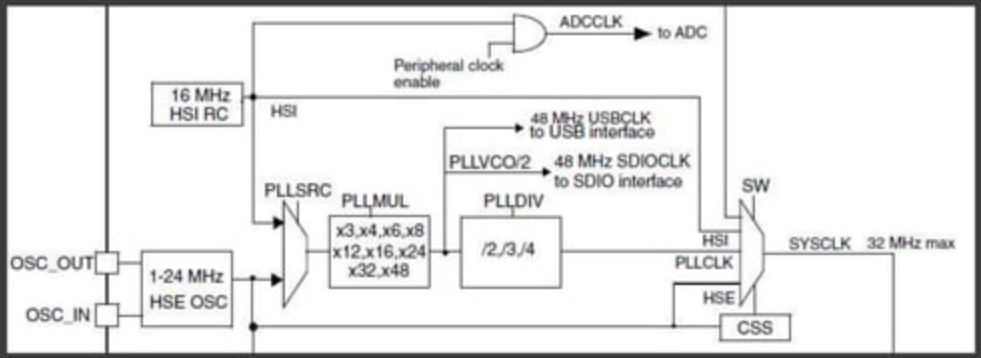
- low-cost (no external components)
- It is used as wake-up clock in low power modes to reduce power consumption and wake-up time.

PLL

The internal PLL can be clocked by the HSI RC or HSE crystal. It is used to drive the system clock and to generate the 48 MHz clock for the USB peripheral



- The PLL input clock frequency must be between 2 and 24 MHz.



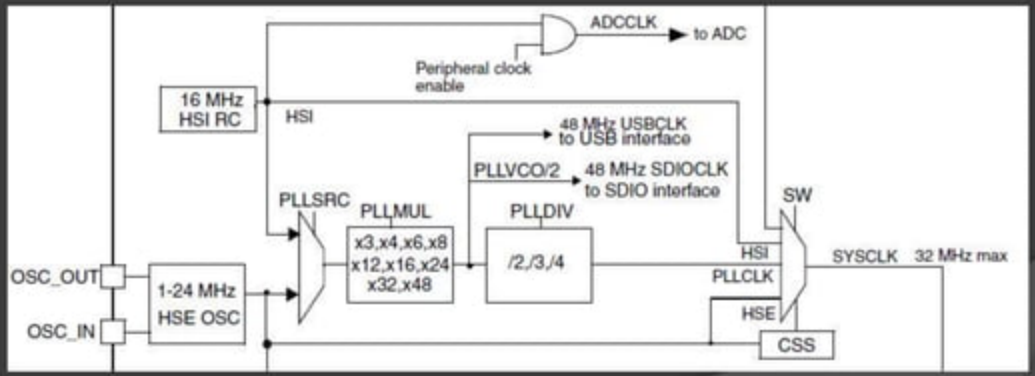
- PLL VCO clock (defined byhe PLL multiplication factor) must be programmed to output a 96 MHz frequency. This is required to provide a 48 MHz clock to the USB or SDIO (SDIOCLK or USBCLK =PLLVCO/2).

System clock (SYSCLK) selection

- A switch from one clock source to another occurs only if the target clock source is ready
- Status bits in the RCC_CR register indicate which clock(s) is (are) ready and which clock is currently used as system clock.

Clock security system (CSS)

•If a failure is detected on the HSE clock, this oscillator is automatically disabled and an interrupt is generated to inform the software about the failure (Clock Security System Interrupt, CSSI)



CSS

- If the HSE oscillator is used directly or indirectly as the system clock
- A detected failure causes a switch of the system clock to the MSI oscillator and the disabling of the HSE

Clock-out capability

- The microcontroller clock output (MCO) capability allows the clock to be output onto the external MCO pin (PA8)